Exam 1

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[6%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(2%) a) Determine the unsigned binary, octal, hexadecimal, and BCD representations of the number 49_{10}.

2|49
2|24 1
2|12 0
2|6 0
2|3 0
2|1 1
0 1

Binary: 110001
Octal: 61
Hex: 31
BCD: 0100 1001

(2%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -73_{10}.

2|73
2|36 1
2|18 0
2|9 0
2|4 1
2|2 0
2|1 0
0 1

0100 1001

Signed Mag: 1100 1001
1's Comp: 1011 0110
2's Comp: 1011 0111

(2%) c) What is $49_{10} - 73_{10}$ in 8-bit 2's complement? Remember that you must **show <u>all</u> work.**

$(49_{10}-73_{10})_2$: 1110 1000

49 0011 0001
+(-73) 1011 0111
-24 1110 1000

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[10%] 2. Answer the following questions given the below **truth table** with inputs W, X and Y and output Z.

W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(2%) a) Write the corresponding **minterm** (i.e., **canonical** sum of products CSOP) –**or**– **maxterm** (i.e., **canonical** product of sums CPOS) equation for Z (one or the other, but not both).

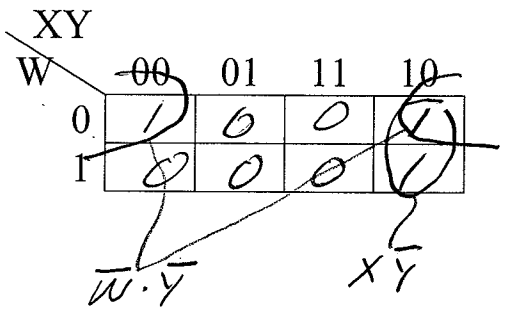
minterms (CSOP) $Z = \overline{W}\cdot\overline{X}\cdot\overline{Y} + \overline{W}\cdot X\cdot\overline{Y} + W\cdot X\cdot\overline{Y}$

maxterms (CPOS) $Z = (W+X+\overline{Y})\cdot(W+\overline{X}+\overline{Y})\cdot(\overline{W}+X+Y)\cdot(\overline{W}+X+\overline{Y})\cdot(\overline{W}+\overline{X}+\overline{Y})$

Which did you write above? (circle one): Minterms (CSOP) Maxterm (CPOS)

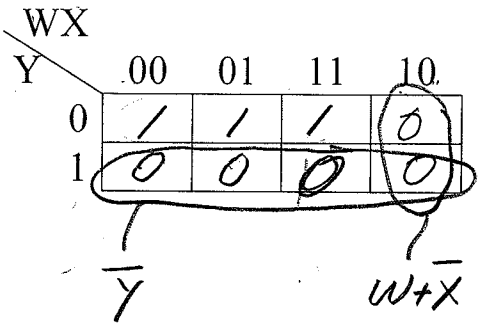
(1%) b) Completely fill in the K-map (to the right) with 1's and 0's (no blanks).

(2%) c) With the K-map to the right, find the minimum sum of products (MSOP) solution. (Label each grouping with the appropriate expression and then write the total equation. Use proper lexical ordering; *i.e., /A before A, A before B, & D_3 before D_2.*)



$Z_{MSOP} = \overline{W}\cdot\overline{Y} + X\cdot\overline{Y}$

(3%) d) Completely fill in the K-map (to the right) with 1's and 0's (no blanks) and find the minimum product of sums (MPOS) solution. **Note**: The order of the signals in the K-map has been changes! (WX is on top)



$Z_{MPOS} = (\overline{W}+X)\cdot\overline{Y}$

(1%) e) Are Z_{MSOP} and Z_{MPOS} equivalent expressions? Why?

Circle One: (Yes (equivalent)) No (not equivalent)

Same truth table (with no don't cares used) you can also prove algebraically that they are equal.

(1%) f) Which solutions is less costly (in gates) and why? **Circle One**: MSOP (MPOS)

MSOP: 2 ANDs, 2 inverters, 1 OR
MPOS: 1 AND, 2 inverters, 1 OR

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[10%] 3. Using any technique you desire, simplify the following equation. Give the result as a minimum sum of products (MSOP).

B & C (don't care)

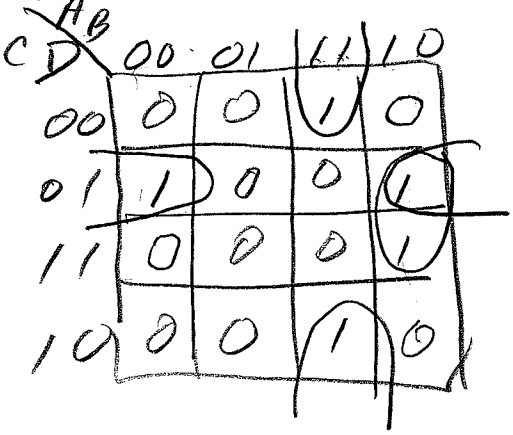
1 0 0 0 0 0 1 1 0 0 1 1 0 1 0

$$Y = (\overline{A} + B + C + D) \bullet (A + B + \overline{C} + \overline{D}) \bullet (A + D) \bullet (\overline{B} + \overline{D}) \bullet (B + \overline{C} + D)$$

It's easier to use a K-map

A, C don't care

A don't care



$Y_{MSOP} = A \cdot \overline{B} \cdot D + A \cdot B \cdot \overline{D} + \overline{B} \cdot \overline{C} \cdot D$

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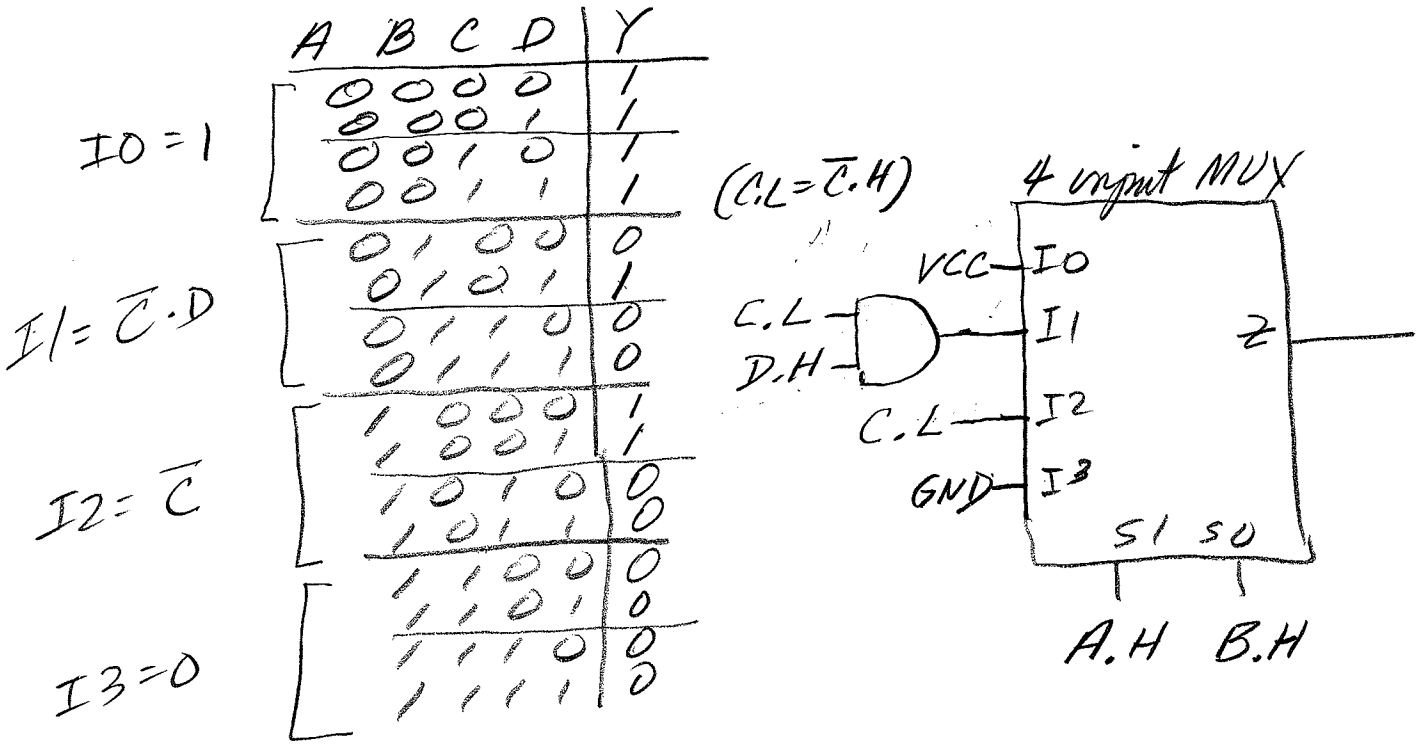
[10%] 4. Using a 4-input multiplexer (i.e., 4-to-1 multiplexer) and any other gates, draw a mixed-logic circuit diagram to realize the following function. (Do **not** attempt to simplify.) Minimize the **number of gates** required. You may choose any activation-levels that will simplify your design.

The 4-to-1 multiplexer has all active-high inputs and an active-high output.

$$Y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C}D + \overline{B}\,\overline{C}$$

Note: you must connect A to S1 of the 4-input mux and B to S0.



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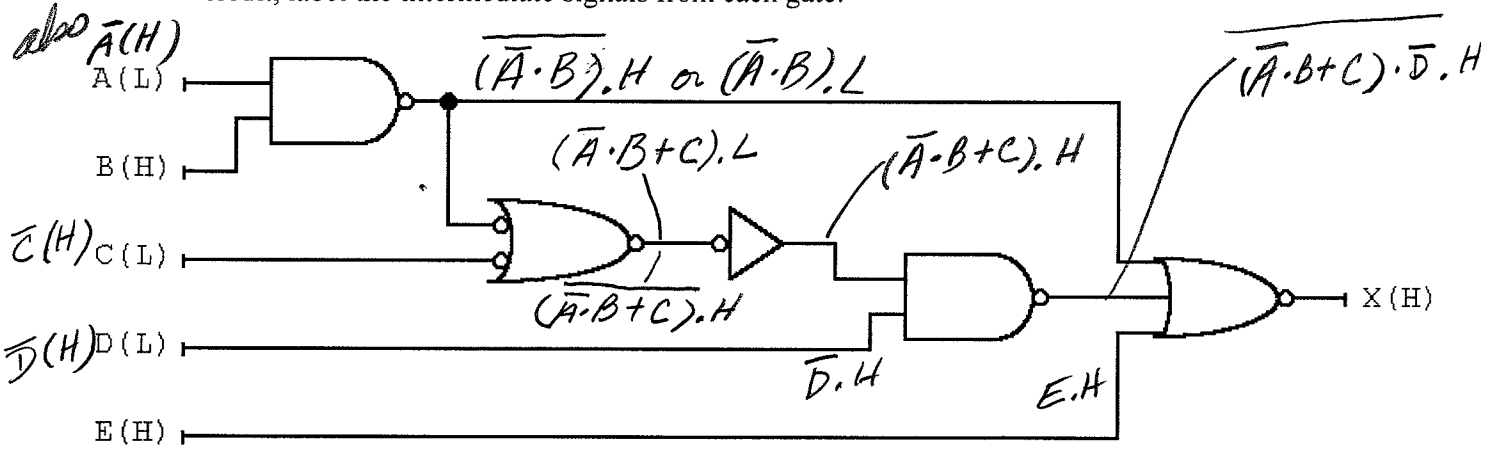
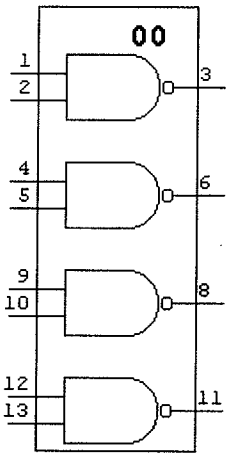
[7%] 5. Determine the equation **directly** implemented with this mixed-logic circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. For partial credit, label the intermediate signals from each gate.

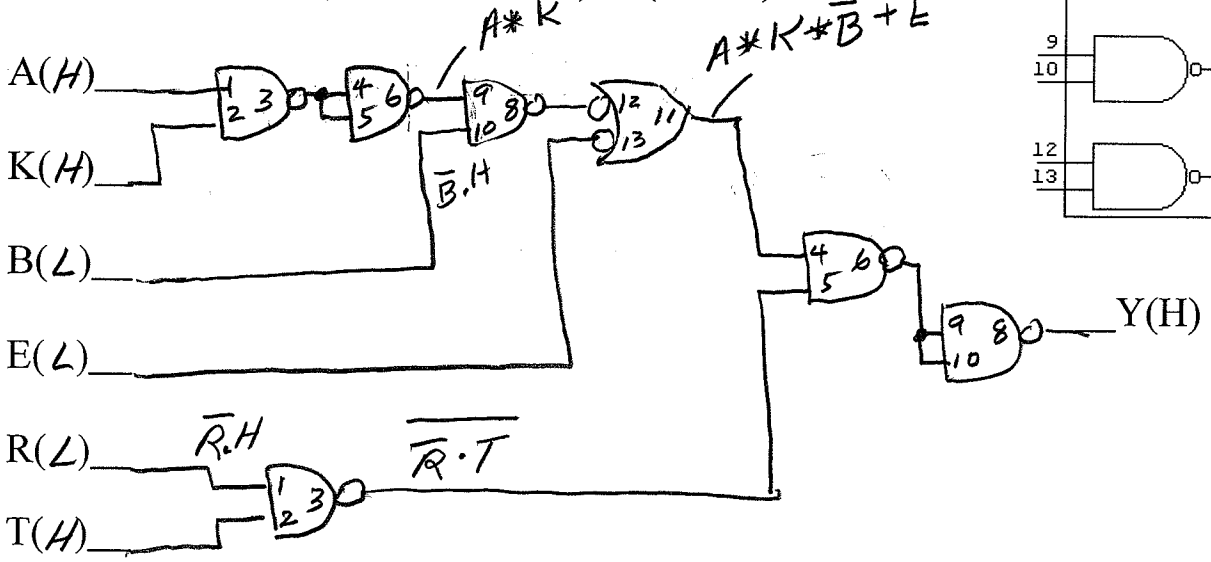


X = $\overline{\overline{A}\cdot B} + \overline{(\bar{A}\cdot B+C)\cdot\bar{D}} + E$

[10%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only gates available on 74'00 chips. (Use the appropriate mixed-logic symbols). **Label** all gates and **pin numbers** as you should be doing in lab. Pick whatever activation levels you want for the inputs, but make the output Y active-high.

Y = (A * K * /B + E) * /(/R * T)





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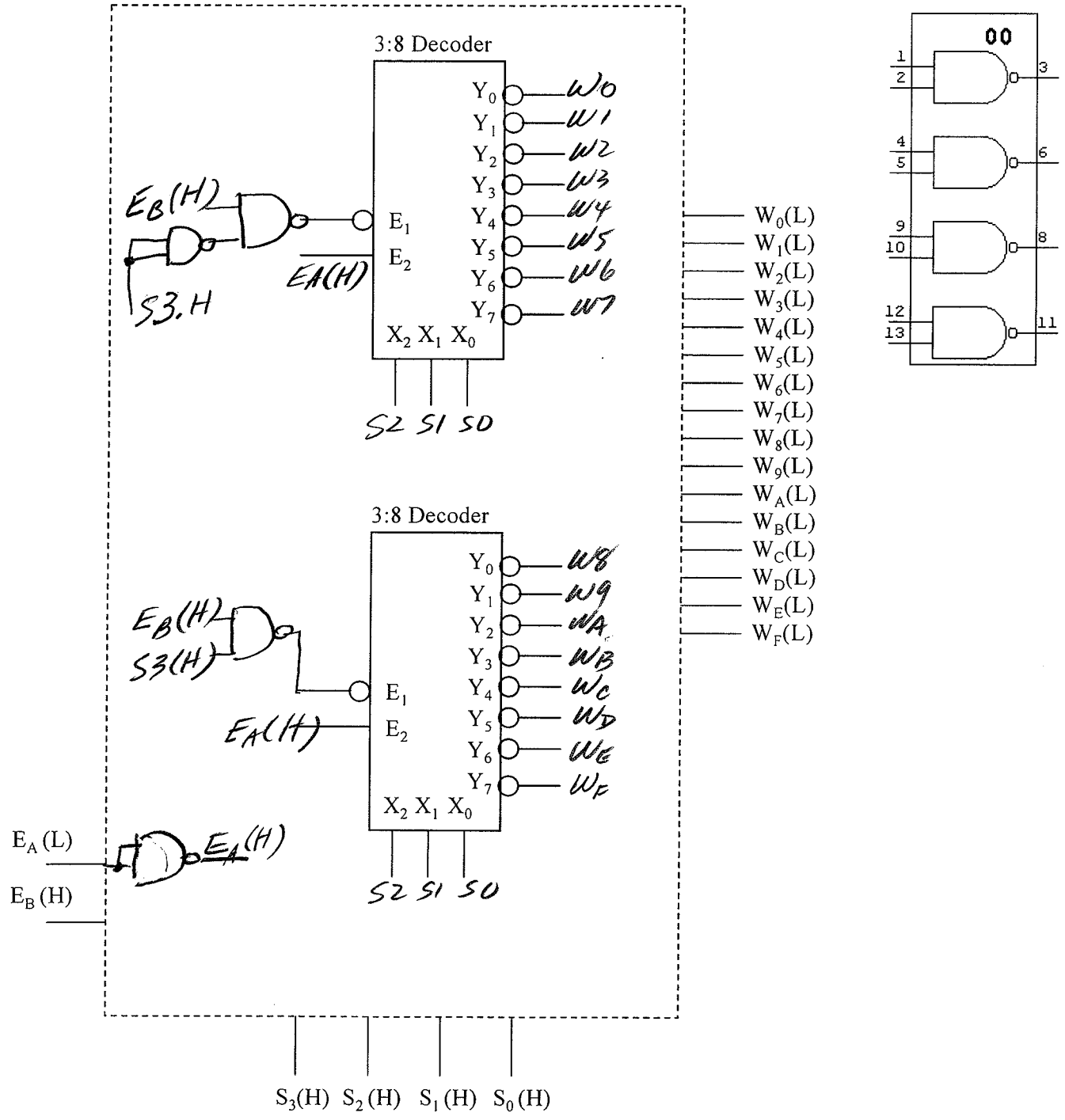
[12%] 7. Given the two 3-to-8 decoders shown (each containing an active-low **and** an active-high enable), create a 4-to-16 decoder, also with an active-high **and** an active-low enable. Use **only** the gates available on **74'00** chips. (A 74'00 is shown.) Add the **minimum** number of additional 74'00 gates required to solve this problem. Note that both E1 and E2 have to be true before the 3:8 Decoder is "on".



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[15%] 8. Answer the following questions about the circuit shown on the next page (p. 9).

(5%) a) What is the logic equation of Z in terms of A, B and C? **Simplify** to an MSOP or an MPOS. **Show all work.** Note that Z is active low Z(L). Also, the inputs are active-high A and B and active-low C.

$Z = \overline{A} + C$

$Q = \overline{S1}\cdot\overline{S0}\cdot D0 + \overline{S1}\cdot S0\cdot D1 + S1\cdot\overline{S0}\cdot D2 + S1\cdot S0\cdot D3$

substitute: $\overline{Z} = \overline{A}\cdot\overline{B}/A + \overline{A}\cdot B\cdot\overline{B} + A\cdot\overline{B}\cdot\overline{C} + A\cdot B\cdot\overline{C}$

($\overline{A}\cdot\overline{B}$ → 0; $\overline{A}\cdot B\cdot\overline{B}$ → 0)

$Z = \overline{A\cdot\overline{B}\cdot\overline{C} + A\cdot B\cdot\overline{C}} = \overline{A\cdot\overline{C}} = \overline{A} + C$

(demorgan's law)

(2%) b) What is the logic equation of D(L) in terms of the inputs A and B (where A is active-high and B is active-low)?

$D = A\cdot\overline{B}$

(8%) c) Complete the following **voltage** table. For the priority encoder, higher numbered inputs have higher priority.

A(H)	B(H)	C(L)	D(L)	Z(L)	Y_0(L)	Y_1(L)
L	L	L	***H***	***L***	***L***	***L***
L	L	H	***H***	***L***	***L***	***L***
L	H	L	***H***	***L***	***H***	***L***
L	H	H	***H***	***L***	***H***	***H***
H	L	L	***L***	***L***	***L***	***L***
H	L	H	***L***	***H***	***L***	***L***
H	H	L	***H***	***L***	***H***	***L***
H	H	H	***H***	***H***	***H***	***H***

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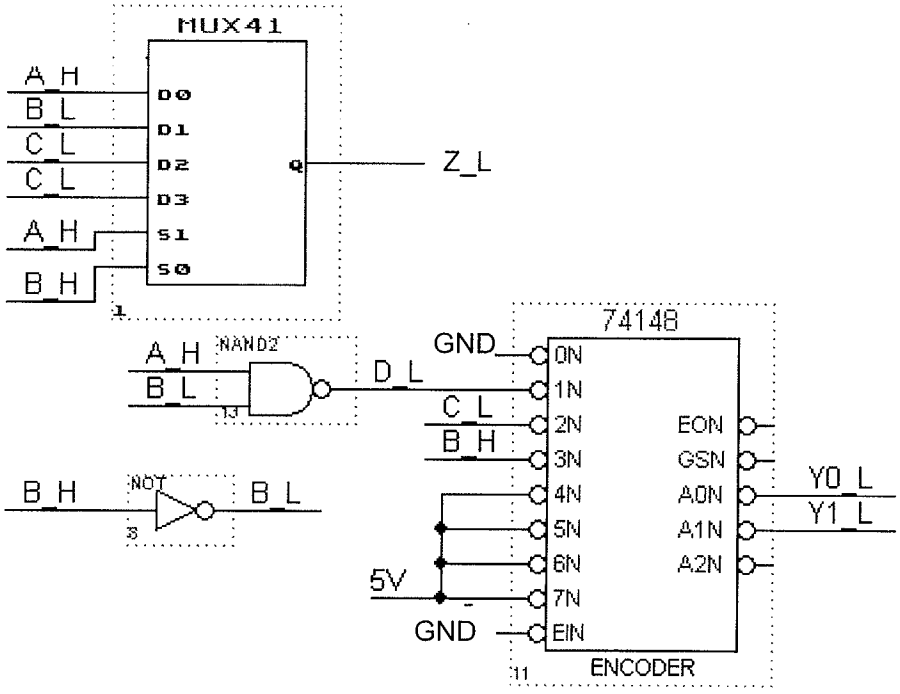
Use this figure for Problem 9 on the previous page (p. 8).



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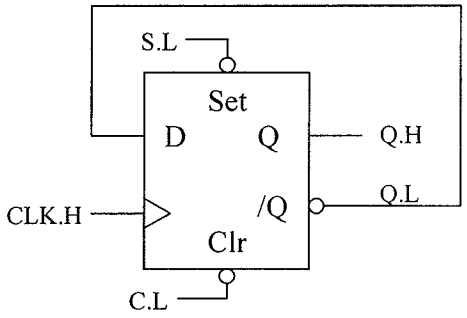
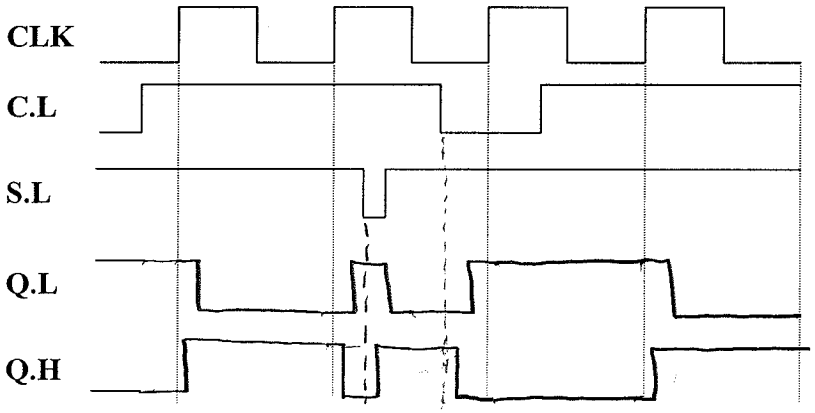
[10%] 9. Given the following circuit, complete the **Voltage** Timing Diagram for Q.L & Q.H below.



Special Notes:
1. Rising edge triggered D Flip-Flop
2. Asynchronous Set & Clear
3. Q.H is initially false

Voltage Timing Diagram. (Fill in Q.L & Q.H.)



Q.H is initially false.

Clearly show all timing delays.

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[10%] 10. Building switches and LEDs

[5%] (a) Shown below are two switches X1 and X2. Complete the design of the two switches to generate two input signals: active low **X1.L** and active high **X2.H**. In other words, make the connections among the switches, resistors, VCC, and GND to produce the two signals.

[5%] (b) Coming out of the digital circuit are two output signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low output Z1.L to an active low LED and the active high output Z2.H to an active high LED. An LED should be lit when the corresponding output is "true".